What have we learned from building the LHC (CMS) DAQ systems.

S. Cittolin PH-CMD. CERN Openlab meeting. 3-4 March 2009

DAQ at LHC overview
CMS systems
Project timeline
CMS experience
Collisions at LHC
The four experiments
Readout and event selection
Trigger levels architecture
Proton-proton collisions at LHC

Collision rate

Collision Rates: \( \sim 10^9 \text{ Hz} \)

Event Selection: \( \sim 1/10^{13} \)
Data detection and event selection

Operating conditions:
- one “good” event (e.g., Higgs in 4 muons) + ~20 minimum bias events

Collision rate

All charged tracks with pt > 2 GeV

Detector granularity: ~ 10^8 cells
Event size: ~ 1 Mbyte
Processing Power: ~ Multi-TFlop

Reconstructed tracks with pt > 25 GeV
Each layer identifies and enables the measurement of the momentum or energy of the particles produced in a collision.
The Experiments

**ATLAS**  Study of **pp** collisions
Tracker: Si (Pixel and SCT), TRT
Calorimeters: LAr, Scintillating Tiles
Muon System: MDT, RPC, TGC, CSC,
Magnets: Solenoid and Toroid

**CMS**  Study of **pp & heavy ion collisions**
Tracker: Si (Pixel, Strips, Discs)
Calorimeters: BGO, Brass Scintillators, Preshower
Muon System: RPC, MDT, CSC,
Supraconducting solenoid

**ALICE**  Study of **heavy ion collisions**
Tracker: Si (ITS), TPC, Chambers, TRD, TOF
Particle Id: RICH, PHOS (scintillating crystals)
RPC, FMD (forward mult.; Si) ZDC (0 degree cal)
Magnets: Solenoid, Dipol

**LHCb**  Study of **CP violation in B decays** (**pp**)
Tracker (Si, Velo), 2 RICH, 4 Tracking stations (Straw-Tubes, Si), SPD (scintill. Pads), Preshower, ECAL (lead scintillator) HCAL (steel scintillator), Muon stations (MWPCs)
40 MHz crossing. Front-end structure

High precision (~ 100ps) timing, trigger and control distribution
40 MHz digitizers and 25ns pipeline readout buffers
40 MHz Level-1 trigger (massive parallel pipelined processors)
Multi-level event selection architecture
CMS front-end readout systems

Acronyms:
- ECAL: Electromagnetic Calorimeter
- HCAL: Hadron Calorimeter
- RPC: Resistive Plate Chambers
- CSC: Cathode Strip Chamber
- DT: Drift Tube
- LV1: Trigger accept
- TTC: Timing, Trigger and Control
- FED: Front-End Driver
- GOL: Gigabit Optical Link
- DDU: Detector Data Unit

Components:
- DDC FED 36: Pixel
- FED 442: Tracker
- DDC FED 50: PreShower
- DDC 60: ECAL
- DDC 24: HCAL
- FED 5: μDT
- DDC FED 3: μRPC
- DDC FED 36: μCSC
- L1-Trigger
Level-1 trigger systems. Pipelines massive parallel

1) Trigger Primitive Generator
Fine grain peak finding
(3888 Logic elements x 116640 crystal data)

2) Pixel Processors
(3888 logic elements x 34992 pixel data)

Trigger based on tracks in external muon detectors that point to interaction region
- Low-p_{T} muon tracks don't point to vertex
  - Multiple scattering
  - Magnetic deflection
- Two detector layers
  - Coincidence in "road"

Detectors:
- RPC (pattern recognition)
- DT (track segment)

RPC pattern recognition
- Pattern catalog
- Fast logic

DT and CSC track finding:
- Finds hit/segments
- Combines vectors
- Formats a track
- Assigns p_{T} value

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Multi-level trigger DAQ architecture

On-line requirements

- Event rate: 1 GHz
- Event size: 1 Mbyte
- Level-1 Trigger input: 40 MHz
- Level-2 Trigger input: 100 kHz
- Mass storage rate: ~100 Hz
- Online rejection: 99.999%
- System dead time: ~%

DAQ design issues

- Data network bandwidth (EVB): ~Tb/s
- Computing power (HLT): ~10 Tflop
- Computing cores: ~10000
- Local storage: ~300 TB

Minimize custom design
Exploit data communication and computing technologies
DAQ staging by modular design (scaling)
## LHC trigger and DAQ summary

<table>
<thead>
<tr>
<th>No. Levels</th>
<th>Level-0,1,2</th>
<th>Event</th>
<th>Readout</th>
<th>HLT Out</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trigger</td>
<td>Rate (Hz)</td>
<td>Size (Byte)</td>
<td>Bandw.(GB/s)</td>
<td>MB/s (Event/s)</td>
</tr>
<tr>
<td>3</td>
<td>LV-1 $10^5$</td>
<td>$1.5 \times 10^6$</td>
<td>4.5</td>
<td>300 $(2 \times 10^2)$</td>
</tr>
<tr>
<td></td>
<td>LV-2 $3 \times 10^3$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>LV-1 $10^5$</td>
<td>$10^6$</td>
<td>100</td>
<td>O$(1000)$ $(10^2)$</td>
</tr>
<tr>
<td>2</td>
<td>LV-0 $10^6$</td>
<td>$3 \times 10^4$</td>
<td>30</td>
<td>40 $(2 \times 10^2)$</td>
</tr>
<tr>
<td>4</td>
<td>Pb-Pb 500</td>
<td>$5 \times 10^7$</td>
<td>25</td>
<td>1250 $(10^2)$</td>
</tr>
<tr>
<td></td>
<td>p-p $10^3$</td>
<td>$2 \times 10^6$</td>
<td></td>
<td>200 $(10^2)$</td>
</tr>
</tbody>
</table>
LHC DAQ architecture

DAQ technologies
DAQ systems at LHC
PS: 1970-80: Minicomputers
Readout custom design
First standard: CAMAC
Software: no OS, Assembler
• kByte/s

p-p/LEP: 1980-90: Microprocessors
HEP proprietary (Fastbus), Industry standards (VME)
Embedded CPU, servers
Software: RTOS, Assembler, Fortran
• MByte/s

LHC: 200X: Networks/Clusters/Grids
PC, PCI, Clusters, point to point switches
Software: Linux, C, C++, Java, Web services
Protocols: TCP/IP, I2O, SOAP,
• TByte/s
A single network cannot satisfy at once all the LHC requirements, therefore present LHC DAQ designs are implemented as multiple (specialized) networks.
Collision rate 40 MHz
Level-1 Maximum trigger rate 100 kHz
Average event size $\approx 1$ Mbyte
Flow control & monitor $\approx 10^6$ Mssg/s
Readout concentrators/links 512 x 4 Gb/s
Event Builder bandwidth max. 2 Tb/s
Event filter computing power $\approx 10$ TeraFlop
Data production $\approx$ Tbyte/day
Processing nodes $\approx$ Thousands

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Two trigger levels

Level-1: Massive parallel processors
40 MHz synchronous
- Particle identification:
  - high pT electron, muon, jets, missing ET
- Local pattern recognition and energy
- Evaluation on prompt macro-granular
- Information from calorimeter and muon detectors

99.99 % rejected: 0.01 Accepted

Level-2: Full event readout into PC farms
100 kHz asynchronous farms
- Clean particle signature
- Finer granularity precise measurement
- Kinematics, effective mass cuts and event topology
- Track reconstruction and detector matching
- Event reconstruction and analysis

99.9 % rejected: 0.1 Accepted

100-1000 Hz. Mass storage
Reconstruction and analysis.
8-fold DAQ structure
Sept. 2008 first events
March 09 Technical Global Run
CMS experience

DAQ project timeline
Industry trends/DAQ
Hardware/Software components
DAQ at Super LHC
<table>
<thead>
<tr>
<th>Year</th>
<th>Event Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1990</td>
<td>Design of experiment</td>
</tr>
<tr>
<td>1992</td>
<td>CMS Letter of Intent</td>
</tr>
<tr>
<td>1994</td>
<td>Technical Design Report</td>
</tr>
<tr>
<td>1996</td>
<td>Event Builder Demonstrators</td>
</tr>
<tr>
<td>1998</td>
<td>8x8 Fiber channel EVB, 32x32 Myrinet EVB</td>
</tr>
<tr>
<td>2000</td>
<td>Trigger Technical Design Report</td>
</tr>
<tr>
<td>2002</td>
<td>Final Design Pre-series</td>
</tr>
<tr>
<td>2004</td>
<td>64x64 Myrinet/Ethernet</td>
</tr>
<tr>
<td>2006</td>
<td>Magnet test Global Run</td>
</tr>
<tr>
<td>2008</td>
<td>Circulating beam Global Run</td>
</tr>
<tr>
<td>2009</td>
<td>Colliding beams</td>
</tr>
</tbody>
</table>

**Research and Development (DRDC)**
- Trigger, Timing and Control distribution (TTC)
- Readout prototypes (FPGA, PC, IOP-200 MB/s)
- Networks (ATM, Fiber Channel, xyz..)
- CMS 2-level triggers design
- FPGA/PC data concentrators
- 8x8 Fiber channel EVB
- 32x32 Myrinet EVB
- 64x64 Ethernet EVB, PC driven
- 64x64 Myrinet/Ethernet

**Construction and commissioning**
- 1024 2 Gb/s D2S Myrinet links and routers
- 8x80x(80x7) GbEthernet EVB/HLT
- 10000 on-line cores

**Lesson 1. 12 yeas of R&D (too much?)**
Lesson 2. Moore law confirmed
Two trajectories

1997 CMS 4x4 FC-EVB

1997 GOOGLE first cluster

2008 Cessy CMS HLT center
10^4 cores, 2 Tb/s maximum bandwidth

2008 One of Google data centers 10^6 cores
### Global Internet traffic (Cisco forecasts)

**US Consumer (PB per month)**

<table>
<thead>
<tr>
<th>Category</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>Web, email, transfer</td>
<td>710</td>
<td>999</td>
<td>1336</td>
<td>1785</td>
<td></td>
</tr>
<tr>
<td>P2P</td>
<td>1747</td>
<td>2361</td>
<td>3075</td>
<td>3981</td>
<td></td>
</tr>
<tr>
<td>Gaming</td>
<td>131</td>
<td>187</td>
<td>252</td>
<td>324</td>
<td></td>
</tr>
<tr>
<td>Video Communications</td>
<td>25</td>
<td>37</td>
<td>49</td>
<td>70</td>
<td></td>
</tr>
<tr>
<td>VoIP</td>
<td>39</td>
<td>56</td>
<td>72</td>
<td>87</td>
<td></td>
</tr>
<tr>
<td>Internet Video to PC</td>
<td>647</td>
<td>1346</td>
<td>2196</td>
<td>3215</td>
<td></td>
</tr>
<tr>
<td>Internet Video to TV</td>
<td>99</td>
<td>330</td>
<td>756</td>
<td>1422</td>
<td></td>
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<tr>
<td>Business</td>
<td>1469</td>
<td>2031</td>
<td>2811</td>
<td>3818</td>
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</tr>
<tr>
<td>Mobile</td>
<td>26</td>
<td>65</td>
<td>153</td>
<td>345</td>
<td></td>
</tr>
<tr>
<td><strong>Total global traffic (Pb/M)</strong></td>
<td><strong>4884</strong></td>
<td><strong>7394</strong></td>
<td><strong>10666</strong></td>
<td><strong>14984</strong></td>
<td></td>
</tr>
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</table>

**Global Internet traffic (Tb/s)**

<table>
<thead>
<tr>
<th>Year</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2014</th>
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<tbody>
<tr>
<td>2007</td>
<td>20</td>
<td>30</td>
<td>40</td>
<td>60</td>
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<tr>
<td>2008</td>
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<td>2009</td>
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<td>2010</td>
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<tr>
<td>2014</td>
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</table>

**Total US traffic (Tb/s)**

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<thead>
<tr>
<th>Year</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2014</th>
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<tbody>
<tr>
<td>2007</td>
<td>3</td>
<td>4</td>
<td>6</td>
<td>8</td>
<td></td>
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<tr>
<td>2008</td>
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<td>2010</td>
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<td>2014</td>
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</table>

**Google US traffic (Tb/s)**

<table>
<thead>
<tr>
<th>Year</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
<td>0.3</td>
<td>0.7</td>
<td>1.5</td>
<td>3</td>
<td></td>
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<tr>
<td>2008</td>
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<td>2009</td>
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<tr>
<td>2010</td>
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<tr>
<td>2014</td>
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</table>

**CMS Maximum bandwidth (Tb/s)**

<table>
<thead>
<tr>
<th>Year</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
<th>2010</th>
<th>2014</th>
</tr>
</thead>
<tbody>
<tr>
<td>2007</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>2</td>
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<tr>
<td>2008</td>
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<td>2009</td>
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<tr>
<td>2010</td>
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<tr>
<td>2014</td>
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</tr>
</tbody>
</table>

**Lesson 3. Will we buy computing power and network bandwidth?**
Readout hardware technologies

Data communication

Custom
6000  1 to 1 Optical trigger primitive readout 1 Gb/s (Rad hard)
60000 1 to 1 Optical analog front-end readout 40 Mb/s (Rad hard)
1000  1 to N Optical fast signal distribution tree 40 MHz
1000  N to 1 Copper Leaves tree signals collection system
800  1 to 1 Copper detector readout LVDS 4 Gb/s links

Proprietary
1024  1 to 1 Optical full duplex data links (Myrinet 2.5 Gb/s)
2056  N to N Optical routers. FED builders (Myrinet)
1024  PCI dual 2.5 Gb/s optical link (Myrinet 2000)

Commercial standard
4120  N to N Copper Ethernet switches (Force10)
800  PCI card quad GbE copper link (Silicom)

Data processing

Custom
All sub-detector digitizers, data concentrator, on detector controls
Trigger processors logic cards

Proprietary
100  Water cooled racks HLT computing rooms (CIAT)

Commercial standard
300  PC Intel Dual-CPU. Front-end VME/PCI controllers (Dell)
700  PC Intel Dual-CPU Dual-Core. DAQ nodes RU-BU (Dell 2950)
900  PC Intel Dual-CPU Quad-Core. High Level Trigger (Dell 1950)
100  PC servers (Dell). 300 Tbyte mass storage
VME and PCI crates, PCI express, Field busses

Lesson 4. Custom/Proprietary/Standards attention
### DAQ costs

**Project construction costs**

<table>
<thead>
<tr>
<th>Category</th>
<th>Quantity</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>R&amp;D, Prototypes and pre-series</td>
<td>120</td>
<td>8%</td>
</tr>
<tr>
<td>120 SuperMicro PCs</td>
<td></td>
<td></td>
</tr>
<tr>
<td>256 port Myrinet switch and interfaces</td>
<td></td>
<td></td>
</tr>
<tr>
<td>512 ports Ethernet switch and interfaces</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Detector readout links</td>
<td>800</td>
<td>4%</td>
</tr>
<tr>
<td>800 Front-end-PCI interfaces</td>
<td></td>
<td></td>
</tr>
<tr>
<td>100 Fast Monitor Modules (FMM)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>D2S 2 Tb/s</td>
<td>300</td>
<td>20%</td>
</tr>
<tr>
<td>300 VME controller PCs and PCI crates</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2048 port Myrinet routers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>1024 dual 2.5 Gb/s Myrinet interfaces</td>
<td></td>
<td></td>
</tr>
<tr>
<td>USC-SCX optical cables</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EVB 100 kHz</td>
<td>640</td>
<td>16%</td>
</tr>
<tr>
<td>640 RUBU Dell 2950 Dual CPU Dual core</td>
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<td></td>
</tr>
<tr>
<td>4120 port GbEthernet switches and interfaces</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HLT 50 kHz</td>
<td>740</td>
<td>10%</td>
</tr>
<tr>
<td>740 Dell 1950 Dual CPU Quad core</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Infrastructures</td>
<td>120</td>
<td>8%</td>
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<tr>
<td>120 Dell 1950 servers</td>
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<td></td>
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<tr>
<td>300 TB local Mass storage. Remote archive link</td>
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<td></td>
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<tr>
<td>Racks W.cooled, Service networks, Controls</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HLT 100 kHz</td>
<td>740</td>
<td>10%</td>
</tr>
<tr>
<td>740 Dell 1950 servers</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total</td>
<td></td>
<td>76%</td>
</tr>
</tbody>
</table>

**Maintenance and Operation costs**

<table>
<thead>
<tr>
<th>Category</th>
<th>Quantity</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Custom and proprietary M&amp;O</td>
<td>25%</td>
<td></td>
</tr>
<tr>
<td>25% spares are acquired for long term</td>
<td></td>
<td></td>
</tr>
<tr>
<td>maintenance of custom designed boards</td>
<td></td>
<td></td>
</tr>
<tr>
<td>and non standard equipment (e.g. Myrinet)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Commercial standards M&amp;O</td>
<td></td>
<td></td>
</tr>
<tr>
<td>HTL PCs are replaced every 3 years</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Data flow PCs, network and storage disks</td>
<td></td>
<td></td>
</tr>
<tr>
<td>are replaced every 4 years. All other servers are replaced every 5 years</td>
<td></td>
<td></td>
</tr>
<tr>
<td>System administration</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dedicated manpower to administrate and</td>
<td></td>
<td></td>
</tr>
<tr>
<td>maintain the PC farms and networks</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Total**

19 76% (of the requested budget in 2003)

**Lesson 5**

Thanks Moore. Should we buy systems and services?
Software technologies

Operating Systems
  Linux SLC4/SLC5, Window

Languages
  C++, Java, Perl, Unix Shells, XML, HTML, Java Script

Databases
  Oracle, MySQL, File System

GUI
  Web Browsers, HTML, DHTML, LabView, Qt, Applets, JFree Chart (Java), ROOT

Protocols
  TCP, HTTP, CGI, I2O (binary for data flow), XDR (binary for monitoring),
  SOAP(XML + binary attachments), SMI, DMI, PVSSII, log4j

Software Maintenance and Documentation
  Quattor, elog, Media wiki, Twiki, CVS, Source Forge, Savannah

DAQ Core framework and components
  System and communication services, Hardware access facilities and device drivers
  Interface to external systems (e.g. DCS, computing services), DAQ monitoring

DAQ applications
  FED builder, Event Builder, HLT framework support, Storage manager, DB support,

Run Control and Monitor System
  Configuration, control and monitoring (> 10000 processes). Interface to operators (GUI, script) and to DCS
  Remote access, security

Detector Controls
  Detector DCS coordination. Common tools development&support, Framework and central DCS system,
  DAQ infrastructure

Lesson 6. Configuration, control and operation of complexity is an issue
Control room

Cessy: Master&Command control room

Fermilab: Remote Operations Center

Meyrin: CMS DQM Center

CR: Any Internet access.....

Security is an issue
SLHC upgrades

Luminosity increase (2012-16) will require
• New front-end electronics and readout links
• Higher level-1 selection power (to maintain 100 kHz max. output)
• Event builder (>10 Tb/s) with an order of magnitude higher

The upgrade programme will include:
• New Front-End digitizers, new rad hard data links and a new timing and trigger distribution system (distribute event type, HLT destination etc.).
• All very front-end systems and selection logic will still be based on custom design. However new telecommunication technologies (e.g. TCA etc.) can be employed to interconnect data concentrators, level-1 logic modules and to interface the detector readout with commercial standards.
• Data to Surface links (10 Tb/s) has to be replaced (2005 proprietary technology life time and 10 time the speed). Likely with standards e.g. 1000x10Gb/s data links (not yet a Moore law for data links)
• Event data fragment will be tagged with trigger type and HLT destination. Event builder and High Level Trigger will be embedded in an single data network (real-time internet clusters/grid like?) which includes local/central data archives and off-line

Lesson 7. the best DAQ R&D is the completion and operation of the current system
Lessons

1. 12 years of R&D (too much?)
   the project has lasted more or less a man generation from design to implementation...

2. Moore law confirmed

3. Will we buy computing power and network bandwidth?
   New kind of commodities. CPU power, memory, mass storage and bandwidth are becoming commercial products..

4. Custom/Standards attention
   Pay attention to maintenance and replacement issues. Survey new standards in the field of telecommunication, server packages, data centers, cooling etc.

5. Less cost, thanks Moore. Buy more from services in the future?
   The process of procurement, installation and commissioning of the last HLT farm took about 10 months (because administrative rules, tender, reliability of components etc.). System management and maintenance for Cluster, Network and Database can be centralized?

6. Configuration and control of complexity is an issue
   Data taking efficiency depends on the real-time system performances but also on the prompt handling of on-line resources. E.g. all experiments need long time (minutes) to cold-start and configure their DAQ system (>10000 processes), Fault tolerant systems, fast recovery etc....
   Distributed control rooms. Master, command, monitor and security

7. DAQ best R&D is the completion and operation of the current system
   The upgrade will be mainly upgrade of network and servers following the M&O expenditure profile. Real new improvement will come from Point 5 issues and the operation experience of the current system
extra
DAQ data flow and computing model

Event rate Level-1

DAQ-HLT input

HLT output

S. Cittolin. CERN/CMS
### CMS design parameters and DAQ requirements

#### Detectors

<table>
<thead>
<tr>
<th>Detector</th>
<th>Channels</th>
<th>Control</th>
<th>Ev. Data</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pixel</td>
<td>60000000</td>
<td>1 GB</td>
<td>50 (kB)</td>
</tr>
<tr>
<td>Tracker</td>
<td>10000000</td>
<td>1 GB</td>
<td>650</td>
</tr>
<tr>
<td>Preshower</td>
<td>145000</td>
<td>10 MB</td>
<td>50</td>
</tr>
<tr>
<td>ECAL</td>
<td>85000</td>
<td>10 MB</td>
<td>100</td>
</tr>
<tr>
<td>HCAL</td>
<td>14000</td>
<td>100 kB</td>
<td>50</td>
</tr>
<tr>
<td>Muon DT</td>
<td>200000</td>
<td>10 MB</td>
<td>10</td>
</tr>
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<td>Muon RPC</td>
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<td>Muon CSC</td>
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<tr>
<td>Trigger</td>
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<td>16</td>
</tr>
</tbody>
</table>

- **Event size**: 1 Mbyte
- **Max LV1 Trigger**: 100 kHz
- **Online rejection**: 99.999%
- **System dead time**: ~ %

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