Intel News Release

Intel Unveils New Product Plans for High-Performance Computing

Intel® Many Integrated Core Chips to Extend Intel's Role in Accelerating Science and Discovery

NEWS HIGHLIGHTS

- The first product codenamed "Knights Corner" will target Intel's 22nm process and use Moore's Law to scale to more than 50 Intel cores.
- Intel® Xeon® processors and Intel® Many Integrated Core architecture-based products to share common tools, software algorithms and programming techniques.
- Products build upon Intel's history of many-core related research including Intel's "Larrabee" program and Single-chip Cloud Computer.
- The share of the TOP500 list that features Intel processors grows to 408 systems, nearly 82 percent.

SANTA CLARA, Calif. and HAMBURG, Germany, May 31, 2010 - During the International Supercomputing Conference (ISC), Intel Corporation announced plans to deliver new products based on the Intel® Many Integrated Core (MIC) architecture that will create platforms running at trillions of calculations per second, while also retaining the benefits of standard Intel processors.

Targeting high-performance computing segments such as exploration, scientific research and financial or climate simulation, the first product, codenamed "Knights Corner," will be made on Intel's 22-nanometer manufacturing (nm) process – using transistor structures as small as 22 billionths of a meter – and will use Moore's Law to scale to more than 50 Intel processing cores on a single chip. While the vast majority of workloads will still run best on award-winning Intel® Xeon® processors, Intel® MIC architecture will help accelerate select highly parallel applications.

Industry design and development kits codenamed "Knights Ferry" are currently shipping to select developers, and beginning in the second half of 2010, Intel will expand the program to deliver an extensive range of developer tools for Intel MIC architecture. Common Intel software tools and optimization techniques between Intel MIC architecture and Intel Xeon processors will support diverse programming models that will place unprecedented performance in the hands of scientists, researchers and engineers, allowing them to increase their pace of discovery and preserve their existing software investments. The Intel® MIC architecture is derived from several Intel projects, including "Larrabee" and such Intel Labs research projects as the Single-chip Cloud Computer.

"The CERN openlab team was able to migrate a complex C++ parallel benchmark to the Intel MIC software development platform in just a few days," said Sverre Jarp, CTO of CERN openlab. "The familiar hardware programming model allowed us to get the software running much faster than expected."

"Intel's Xeon processors, and now our new Intel® Many Integrated Core architecture products, will further push the boundaries of science and discovery as Intel accelerates solutions to some of humanity's most challenging problems," said Kirk Skaugen, vice president and general manager of Intel's Data Center Group. "The Intel® MIC architecture will extend Intel's leading HPC products and solutions that are already in nearly 82 percent of the world's top supercomputers. Today's investments are indicative of Intel's growing commitment to the global HPC community."

TOP500

The 35th edition of the TOP500 list, which was announced at ISC, shows that Intel continues to be the platform of choice in high-performance computing, with 408 systems, or nearly 82 percent, powered by Intel processors. More

Photography

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Kirk Skaugen, vice president and general manager of Intel's Data Center Group during his keynote at the international Supercomputing Conference in Hamburg, Germany. Skaugen announced plans to deliver new products based on the Intel® Many Integrated Core (MIC) architecture that will create platforms running at trillions of calculations per second, while also retaining the benefits of standard Intel processors. (JPG 3.6MB)

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Kirk Skaugen, vice president and general manager of Intel's Data Center Group holds a 22nm SRAM test wafer during his keynote at the international Supercomputing Conference in Hamburg, Germany. Skaugen announced plans to deliver new products based on the Intel® Many Integrated Core (MIC) architecture that will create platforms running at trillions of calculations per second, while also retaining the benefits of standard Intel processors. (JPG 6MB)

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Kirk Skaugen, vice president and general manager of Intel's Data Center Group holding the 'Knights Ferry' Intel Many Integrated Core (MIC) architecture-based development card during his keynote at the international Supercomputing Conference in Hamburg, Germany. Skaugen announced plans to deliver new products based on the Intel MIC architecture that

than 90 percent of quad-core-based systems use Intel processors, with the Intel® Xeon® 5500 series processor nearly doubling its presence with 186 systems. Intel chips also power three systems in the top 10, and four out of five new entrants in the top 30. Seven systems contain the recently announced Intel® Xeon® 5600 series processor, codenamed "Westmere-EP," and two systems are powered by the new Intel® Xeon® 7500 series processor, codenamed "Nehalem-EX."

The Intel Xeon processor 5600 series is playing the vital role in the highest-ranked system from China in the history of the Top500. The No. 2 system, located at the National Supercomputing Center (NSCS) in Shenzhen, reached 1.2 petaflops on the Linpack benchmark with a Dawning TC3600*. NSCS is a hub for research and innovation in China.

The semi-annual TOP500 list of supercomputers is the work of Hans Meuer of the University of Mannheim, Erich Strohmaier and Horst Simon of the U.S. Department of Energy's National Energy Research Scientific Computing Center, and Jack Dongarra of the University of Tennessee. The complete report is available at www.top500.org.

New Exascale Lab

To meet the growing challenge of running large-scale simulations in the multi petaflops and exaflops range of computing, Intel, Forschungszentrum Julich (FZJ) and ParTec will announce a multi-year commitment to create the ExaCluster Laboratory (ECL) at Julich. The lab will develop key technologies, tools and methods to power multi petaflops and exaflops machines, focusing on the scalability and resilience of those systems. ECL will become the latest member of Intel Labs Europe, a network of research and innovation centers spanning Europe.

A webcast of Kirk Skaugen's International Supercomputing 2010 keynote presentation will be available here: lecture2go.uni-hamburg.de/live.

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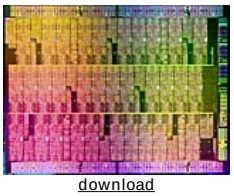
will create platforms running at trillions of calculations per second, while also retaining the benefits of standard Intel processors. (JPG 3.7MB)



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Die shot of Aubrey Isle silicon. Aubrey Isle is the codename of the silicon chip included the 'Knights Ferry' Intel Many Integrated Core (MIC) architecture development platform. (JPG 3.9MB)

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