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Many Integrated Core (MIC) Architecture - Advanced

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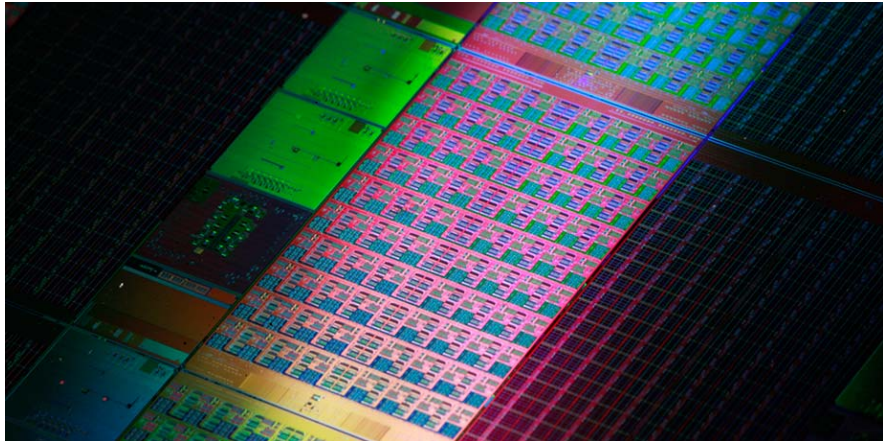
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Processor speed jumps exponentially

Intel® Many Integrated Core (Intel® MIC) architecture ushers in a new era of supercomputing speed, performance, and compatibility. Now developers can create platforms running at trillions of calculations per second using fast and familiar Intel® Xeon® processors and co-processors based on the new architecture.

This is an exponential leap forward. Now that supercomputers have broken the petaflop barrier, Intel already foresees a combination of many Intel® MIC processors surpassing the next big milestone: the exaflop or 1,000 petaflop barrier.



Getting started with highly parallel applications

The first Intel MIC products target segments and applications that use highly parallel processing, including:

- High Performance Computing (HPC)
- Workstation
- Data Center

The MIC architecture utilizes a high degree of parallelism in smaller, lower-power, and single-threaded performance Intel® processor cores. The result is higher performance on highly parallel applications.

While relatively few specialized applications today are highly parallel, these applications address a wide range of important issues—ranging from climate change simulations and genetic analysis, to investment portfolio risk management and the search for new sources of energy.

Knights Corner launches the technology

The first product based on Intel® MIC architecture targets HPC segments such as oil exploration, scientific research, financial analyses, and climate simulation, among many others. It's codenamed Knights Corner, and Intel is building it on 22-nanometer manufacturing process using transistor structures as small as 22 billionths of a meter. It will scale to more than 50 Intel processing cores on a single chip.

Using standard programming languages

Intel® MIC products give developers a key advantage: They run on standard, existing programming tools and methods.

Intel® MIC architecture combines many Intel® CPU cores onto a single chip. Developers can program these cores using standard C, C++, and FORTRAN source code. The same program source code written for Intel® MIC products can be compiled and run on a standard Intel® Xeon processor. Familiar programming models remove developer-training barriers, allowing the developer to focus on the problems rather than software engineering.

Consider the example of CERN OpenLab, the European Organization for Nuclear Research. This group took advantage of the Knights Ferry kit (See explanation below) to migrate a complex benchmark written in C++ code to the new architecture in just a few days. According to Sverre Jarp, CTO of the CERN open lab, "The familiar hardware programming model allowed us to get the software running much faster than expected."

Knights Ferry supports the launch

This design and development kit helps select software and hardware developers prepare for Knights Corner. In late 2010, Intel expanded the kit to include a broader range of developer tools for the Intel MIC architecture. As a result, it works more in concert with Intel® Xeon processors to support diverse programming models. Knights Ferry is already placing unprecedented performance in the hands of scientists, researchers, and engineers.

The product of three research initiatives

The MIC project draws upon the great work of three research streams:

[The 80-core Tera-scale research chip program](#)


[The single-chip cloud computer initiative](#)


The Larrabee many-core visual computing project

The result is a fundamentally new architecture that uses the same tools, compilers, and libraries as the Intel® Xeon processors. Because [Intel processors are used in over 80% of the world's supercomputers](#) programmers can continue to work in familiar territory when creating software for the MIC architecture.

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