What have we learned from building the LHC (CMS) DAQ systems.

S. Cittolin PH-CMD. CERN Openlab meeting. 3-4 March 2009 DAQ at LHC overview CMS systems Project timeline CMS experience



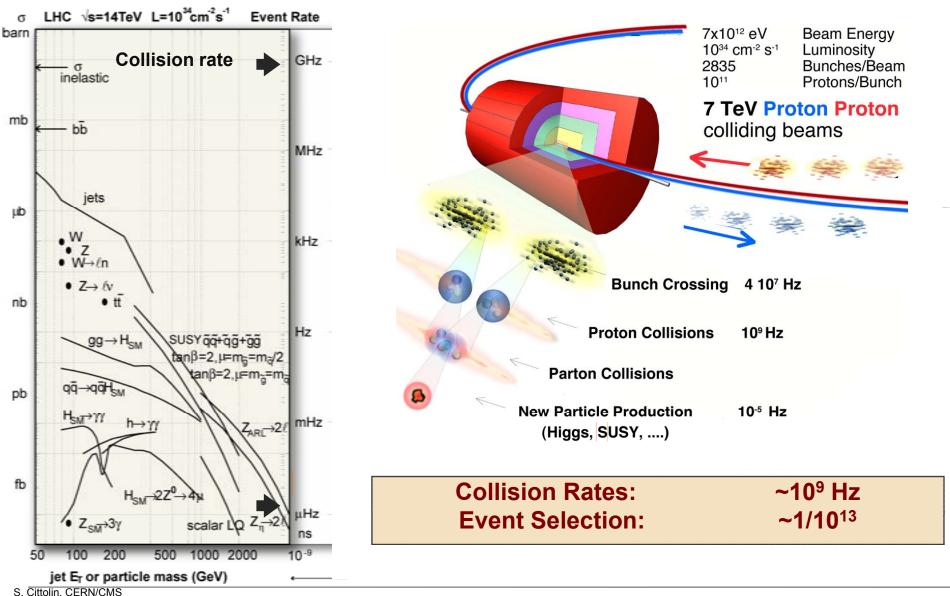
Trigger and DAQ overview



Collisions at LHC The four experiments Readout and event selection Trigger levels architecture



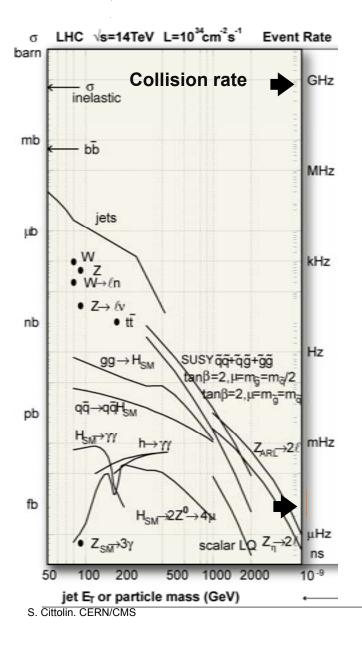
Proton-proton collisions at LHC





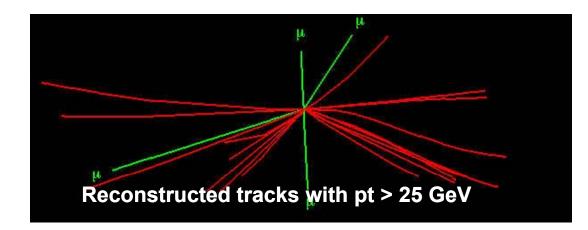
Data detection and event selection







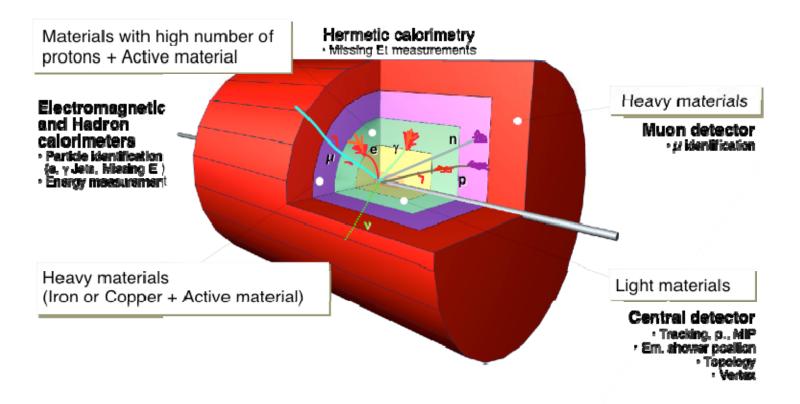
Detector granularity	~ 10 ⁸ cells
Event size:	~ 1 Mbyte
Processing Power:	~ Multi-TFlop





General purpose p-p detectors at LHC





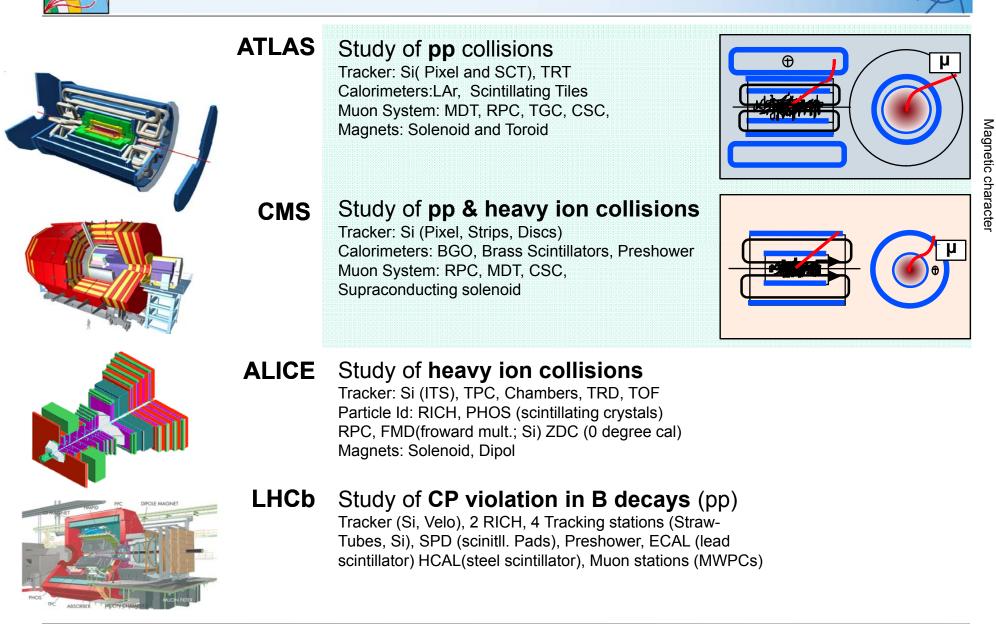
Each layer identifies and enables the measurement of the momentum or energy of the particles produced in a collision

5



The Experiments

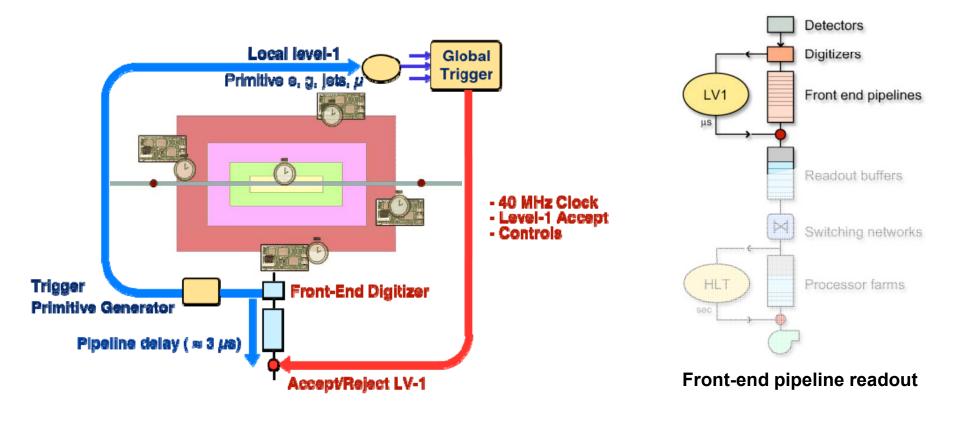




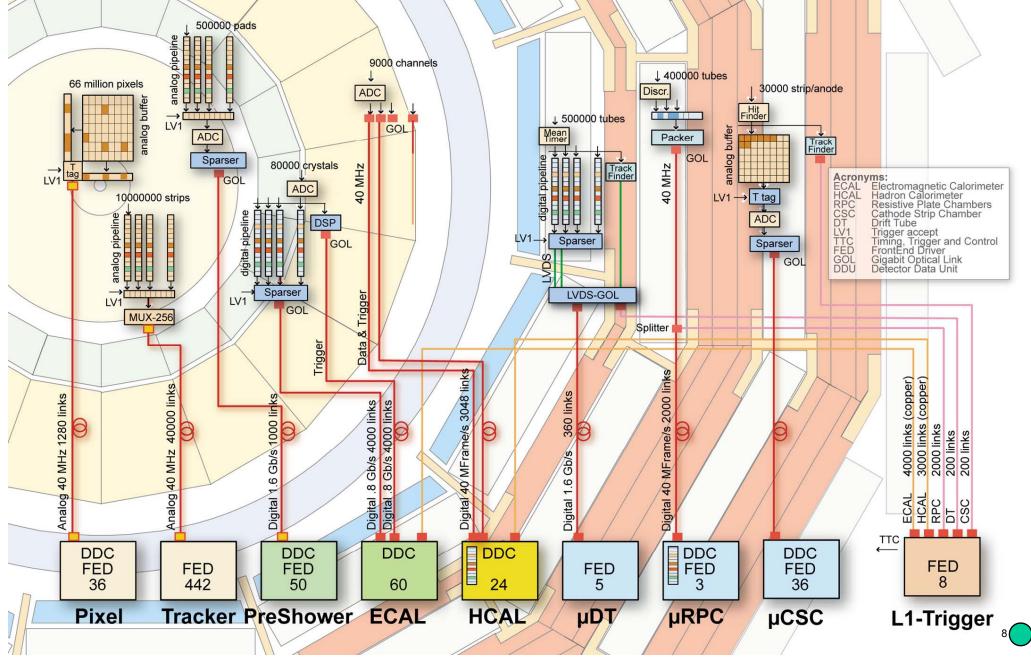




High precision (~ 100ps) timing, trigger and control distribution
40 MHz digitizers and 25ns pipeline readout buffers
40 MHz Level-1 trigger (massive parallel pipelined processors)
Multi-level event selection architecture

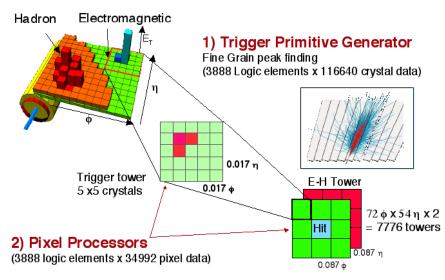


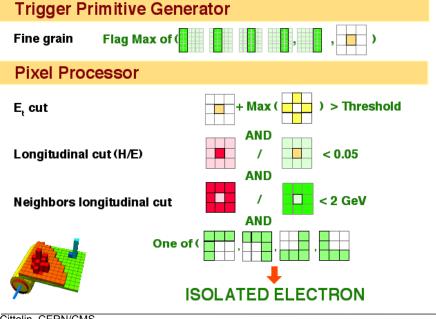
CMS front-end readout systems





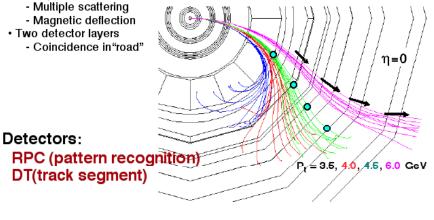
Level-1 trigger systems. Pipelines massive parallel



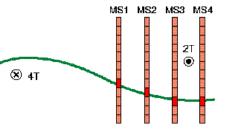


Trigger based on tracks in external muon detectors that point to interaction region

Low-p_↑ muon tracks don't point to vertex

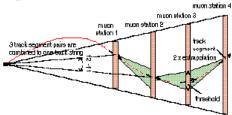


- **RPC** pattern recognition
- Pattern catalog
- Fast logic



DT and CSC track finding:

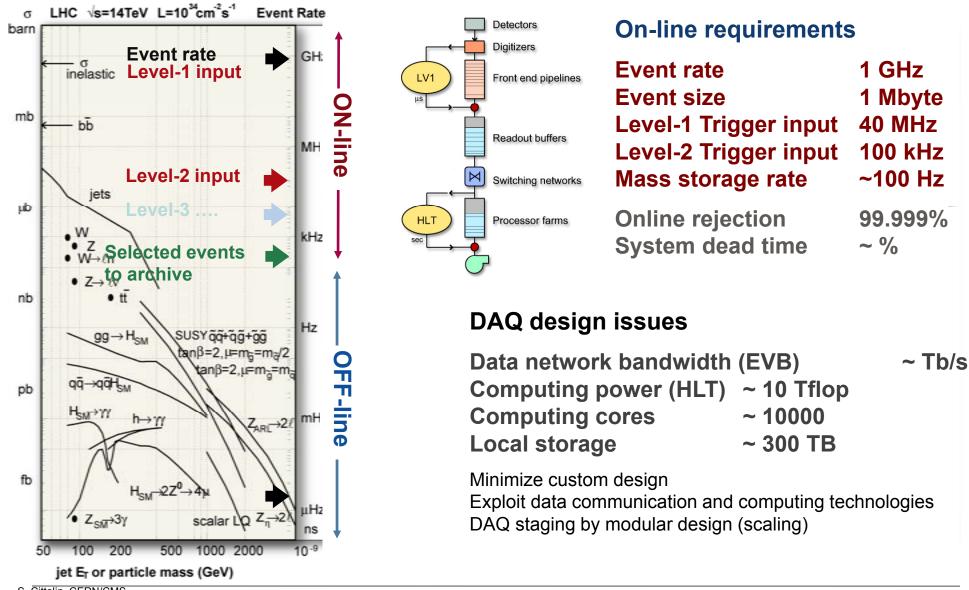
- Finds hit/segments
- Combines vectors
- Formats a track
- Assigns p, value





Multi-level trigger DAQ architecture







LHC trigger and DAQ summary



	No.Levels Trigger	Level-0,1,2 Rate (Hz)	Event Size (Byte)	Readout Bandw.(GB/s)	HLT Out MB/s (Event/s)
	3	LV-1 10⁵ LV-2 3x10³	1.5x10 ⁶	4.5	300 (2x10 ²)
	2	LV-1 10 5	10 ⁶	100	O(1000) (10 ²)
	2	LV-0 10 ⁶	3x10⁴	30	40 (2x10 ²)
PICE ALCREE PLANE	4	_{Рь-Рь} 500 _{р-р} 10 ³	5x10 ⁷ 2x10 ⁶	25	1250 (10 ²) 200 (10 ²)



LHC DAQ architecture

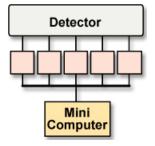


DAQ technologies DAQ systems at LHC



Evolution of DAQ technologies and structures

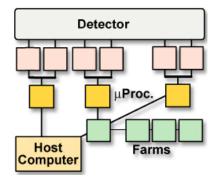




PS:1970-80: Minicomputers

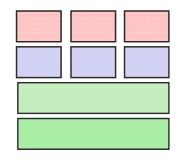
Readout custom design First standard: CAMAC Software: noOS, Assembler • kByte/s

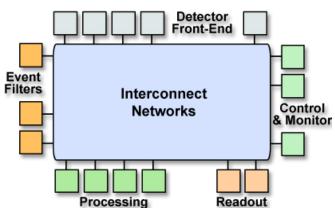
Detector Reacout
Event building
On-line processing



p-p/LEP:1980-90: Microprocessors

HEP proprietary (Fastbus), Industry standards (VME)
Embedded CPU, servers
Software: RTOS, Assembler, Fortran
MByte/s

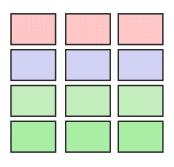




LHC: 200X: Networks/Clusters/Grids

PC, PCI, Clusters, point to point switches Software: Linux, C,C++,Java,Web services Protocols: TCP/IP, I2O, SOAP,

• TByte/s

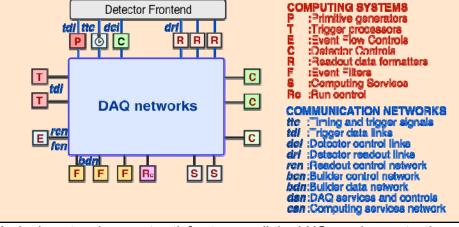




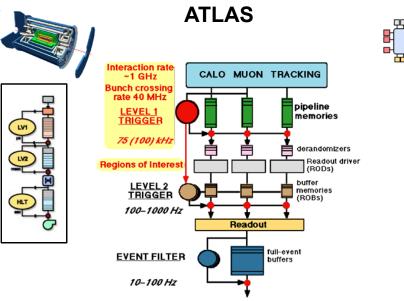
LHC trigger and data acquisition systems

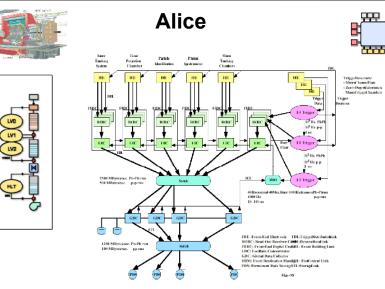


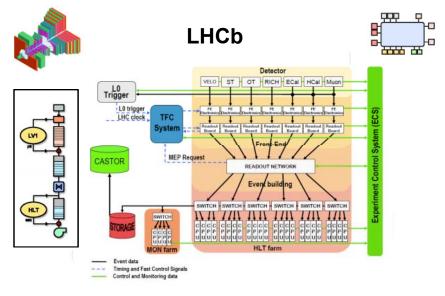
LHC DAQ : A computing&communication network



A single network cannot satisfy at once all the LHC requirements, therefore present LHC DAQ designs are implemented as multiple (specialized) networks

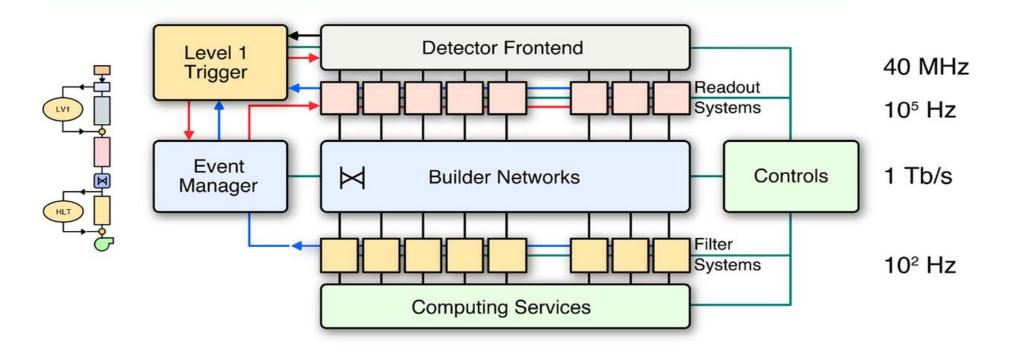








CMS DAQ baseline structure

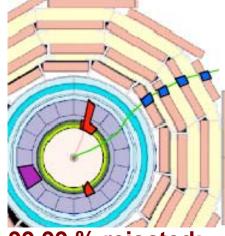


•	40 MHz 100 kHz ≈ 1 Mbyte ≈ 10 ⁶ Mssg/s	Readout concentrators/links Event Builder bandwidth max. Event filter computing power Data production Processing nodes	512 x 4 Gb/s 2 Tb/s ≈ 10 TeraFlop ≈ Tbyte/day ≈ Thousands
---	--	--	---



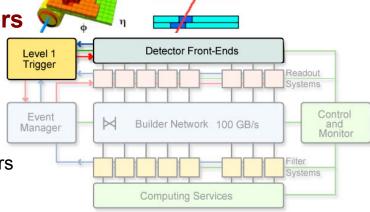
Two trigger levels





Level-1: Massive parallel processors 40 MHz synchronous

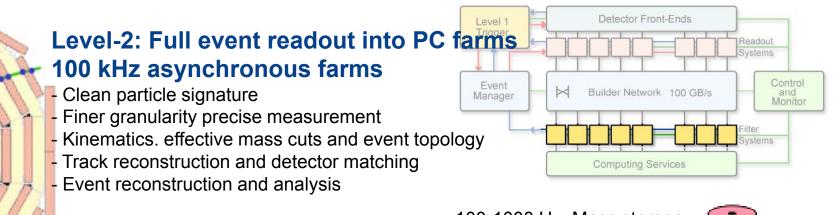
-Particle identification: -high pT electron, muon, jets, missing ET -Local pattern recognition and energy -evaluation on prompt macro-granular -information from calorimeter and muon detectors



99.99 % rejected:

0.01 Accepted

0.1 Accepted

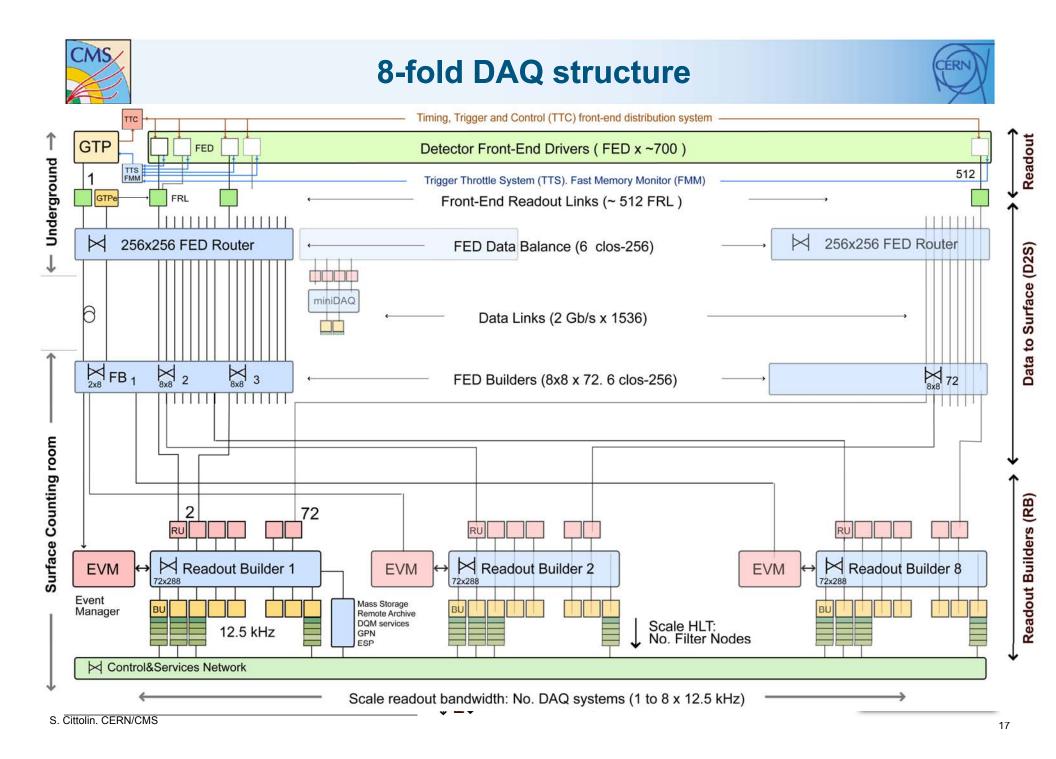


100-1000 Hz. Mass storage Reconstruction and analysis.



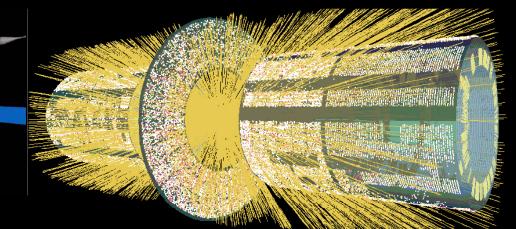
S Cittolin CERN/CMS

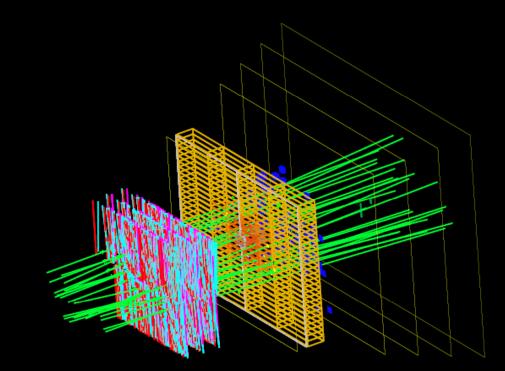
99.9 % rejected:

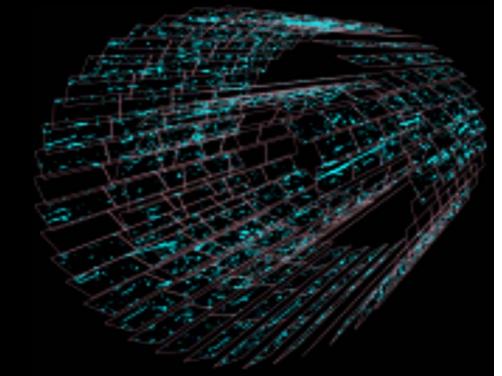


Sept. 2008 first events











March 09 Technical Global Run







CMS experience



DAQ project timeline Industry trends/DAQ Hardware/Software components DAQ at Super LHC



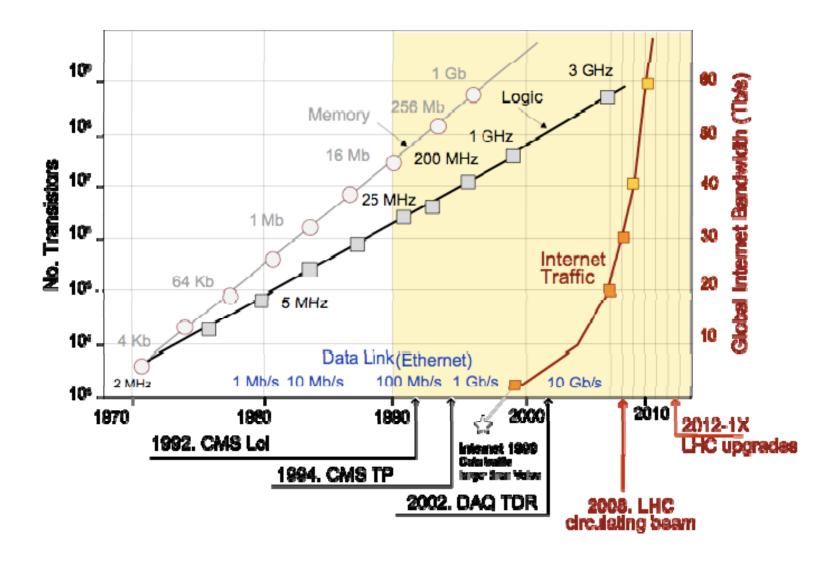
LHC/CMS-DAQ project timeline



1990 Design of experiment	Research and Development (DRDC) Trigger, Timing and Control distribution (TTC)
1992 CMS Letter of Intent	Readout prototypes (FPGA,PC, IOP-200 MB/s) Networks (ATM, Fiber Channel, xyz)
1994 Technical Design Report	CMS 2-level triggers design
1996	Event Builder Demonstrators
1998	FPGA/PC data concentrators 8x8 Fiber channel EVB 32x32 Myrinet EVB
2000 Trigger Technical Design Rep	-
2002 DAQ Technical Design Rep	ort
2004	Final Design Pre-series 64x64 Myrinet/Ethernet
2006 Magnet test Global Run	Construction and commissioning 1024 2 Gb/s D2S Myrinet links and routers 8x80x(80x7) GbEthernet EVB/HLT
2008 Circulating beam Global R	
S. Cittolin. CERN/CMS	2 yeas of R&D (too much?)



Computing and communication trends



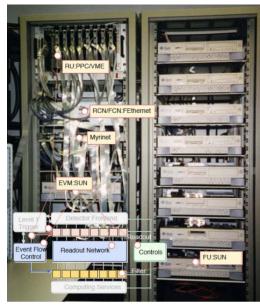
Lesson 2. Moore law confirmed



Two trajectories



1997 CMS 4x4 FC-EVB







1997 GOOGLE first cluster



2008 Cessy CMS HLT center 10⁴ cores, 2 Tb/s maximum bandwidth



2008 One of Google data centers 10⁶ cores





Global Internet traffic (Cisco forecasts)



US Consumer (PB per month) Web, email, transfer P2P Gaming Video Communications VoIP Internet Video to PC Internet Video to TV Business	2007 710 1747 131 25 39 647 99 1469	2008 999 2361 187 37 56 1346 330 2031	2009 1336 3075 252 49 72 2196 756 2811	2010 1785 3981 324 70 87 3215 1422 3818	2014
Mobile	26	65	153	345	
Total global traffic (Pb/M)	4884	7394	10666	14984	
Global Internet traffic (Tb/s)	20	30	40	60	
Total US traffic (Tb/s)	3	4	6	8	
Google US traffic (Tb/s)	0.3	0.7	1.5	3	
CMS Maximum bandwidth (Tb/s)	1	2	2	2	>10

S. Cittolin, CERN/CMS



Readout hardware technologies



Data communication

Custom

6000	1 to 1 Optical trigger primitive readout 1 Gb/s (Rad hard)
60000	1 to 1 Optical analog front-end readout 40 Mb/s (Rad hard)
1000	1 to N Optical fast signal distribution tree 40 MHz
1000	N to 1 Copper Leaves tree signals collection system
800 1 to 1 Cop	per detector readout LVDS 4 Gb/s links
Proprietary	
1024	1 to 1 Optical full duplex data links (Myrinet 2.5 Gb/s)
2056	N to N Optical routers. FED builders (Myrinet)
1024	PCI dual 2.5 Gb/s optical link (Myrinet 2000)

Commercial standard

4120 N to N Copper Ethernet switches (Force10) 800 PCI card guad GbE copper link (Silicom)

Data processing

Custom

All sub-detector digitizers, data concentrator, on detector controls Trigger processors logic cards

Proprietary

100 Water cooled racks HLT computing rooms (CIAT)

Commercial standard

300 PC Intel Dual-CPU. Front-end VME/PCI controllers (Dell)
700 PC Intel Dual-CPU Dual-Core. DAQ nodes RU-BU (Dell 2950)
900 PC Intel Dual-CPU Quad-Core. High Level Trigger (Dell 1950)
100 PC servers (Dell). 300 Tbyte mass storage
VME and PCI crates, PCI express, Field busses

C	M	s/
	4	3
	T	5

DAQ costs



Project construction costs			Maintenance and Operation costs
R&D, Prototypes and pre-series 120 SuperMicro PCs 256 port Myrinet switch and interfaces 512 ports Ethernet switch and interfaces	2	8%	
Detector readout links 800 Front-end-PCI interfaces 100 Fast Monitor Modules (FMM)	1	4%	Custom and proprietary M&O 25% spares are acquired for long term
D2S 2 Tb/s 300 VME controller PCs and PCI crates 2048 port Myrinet routers 1024 dual 2.5 Gb/s Myrinet interfaces USC-SCX optical cables	5	20%	maintenance of custom designed boards and non standard equipment (e.g. Myrinet)
EVB 100 kHz 640 RUBU Dell 2950 Dual CPU Dual core 4120 port GbEthernet switches and interfaces	4	16%	Commercial standards M&O HTL PCs are replaced every 3 years
HLT 50 kHz 740 Dell 1950 Dual CPU Quad core	2.5	10%	Data flow PCs, network and storage disks are replaced every 4 years . All other servers are
Infrastructures 120 Dell 1950 servers 300 TB local Mass storage. Remote archive link Racks W.cooled, Service networks, Controls	2	8%	replaced every 5 years System administration Dedicated manpower to administrate and
HLT 100kHz	2.5	10%	maintain the PC farms and networks
Total	10	76%	(of the requested budget in 2003)



Software technologies



Operating Systems

Linux SLC4/SLC5, Window

Languages

C++, Java, Perl, Unix Shells, XML, HTML, Java Script

Databases

Oracle, MySQL, File System

GUI

Web Browsers, HTML, DHTML, LabView, Qt, Applets, JFree Chart (Java), ROOT

Protocols

TCP, HTTP, CGI, I2O (binary for data flow), XDR (binary for monitoring), SOAP(XML + binary attachments), SMI, DMI, PVSSII, log4j

Software Maintenance and Documentation

Quattor, elog, Media wiki, Twiki, CVS, Source Forge, Savannah

DAQ Core framework and components

System and communication services, Hardware access facilities and device drivers Interface to external systems (e.g. DCS, computing services), DAQ monitoring

DAQ applications

FED builder, Event Builder, HLT framework support, Storage manager, DB support,

Run Control and Monitor System

Configuration, control and monitoring (> 10000 processes). Interface to operators (GUI, script) and to DCS Remote access, security

Detector Controls

Detector DCS coordination. Common tools development&support,Framework and central DCS system,

DAQ infrastr Lesson 6. Configuration, control and operation of complexity is an issue

S. Cittolin. CERN/CMS



Control room



Cessy: Master&Command control room



Meyrin: CMS DQM Center



Fermilab: Remote Operations Center



CR: Any Internet access.....



Security is an issue



SLHC upgrades



Luminosity increase (2012-16) will require

New front-end electronics and readout links
Higher level-1 selection power (to maintain 100 kHz max. output)
Event builder (>10 Tb/s) with an order of magnitude higher

The upgrade programme will include:

•New Front-End digitizers, new rad hard data links and a new timing and trigger distribution system (distribute event type, HLT destination etc.).

•All very front-end systems and selection logic will still be based on custom design. However **new telecommunication technologies** (e.g. TCA etc.) can be employed to interconnect data concentrators, level-1 logic modules and to interface the detector readout with commercial standards.

•Data to Surface links (10 Tb/s) has to be replaced (2005 proprietary technology life time and 10 time the speed). Likely with standards e.g. 1000x10Gb/s data links (not yet a Moore law for data links)

•Event data fragment will be tagged with trigger type and HLT destination. Event builder and High Level Trigger will be **embedded in an single data network** (real-time internet clusters/grid like?) which includes local/central data archives and off-line

Lesson 7. the best DAQ R&D is the completion and operation of the current system



Lessons



1. 12 yeas of R&D (too much?)

the project has lasted more or less a man generation from design to implementation...

2. Moore law confirmed

3. Will we buy computing power and network bandwidth?

New kind of commodities. CPU power, memory, mass storage and bandwidth are becoming commercial products..

4. Custom/Standards attention

Pay attention to maintenance and replacement issues. Survey new standards in the field of telecommunication, server packages, data centers, cooling etc.

5. Less cost, thanks Moore. Buy more from services in the future?

The process of procurement, installation and commissioning of the last HLT farm took about 10 months (because administrative rules, tender, reliability of components etc.). System management and maintenance for Cluster, Network and DataBase can be centralized?

6. Configuration and control of complexity is an issue

Data taking efficiency depends on the real-time system performances but also on the prompt handling of online resources. E.g. all experiments need long time (minutes) to cold-start and configure their DAQ system (> 10000 processes), Fault tolerant systems, fast recovery etc....

Distributed control rooms. Master, command, monitor and security

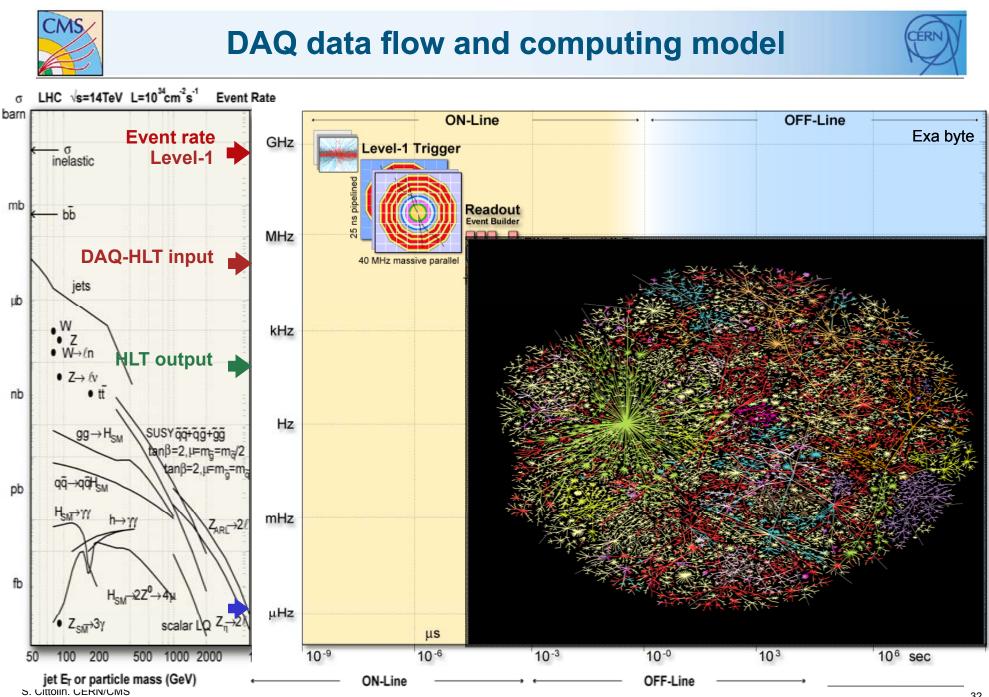
7. DAQ best R&D is the completion and operation of the current system

The upgrade will be mainly upgrade of network and servers following the M&O expenditure profile. Real new improvement will come from Point 5 issues and the operation experience of the current system







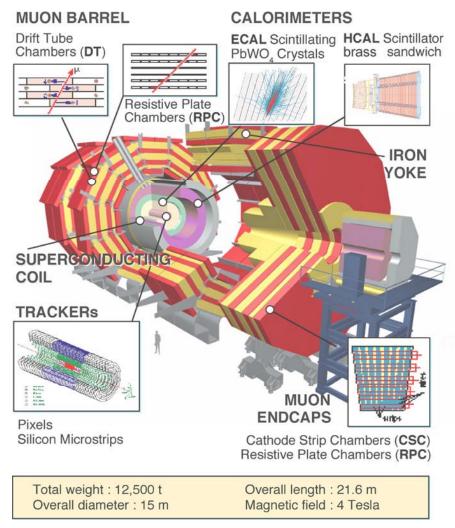




CMS design parameters and DAQ requirements



Detectors



Detector	Channels	Control	Ev. Data
Pixel	6000000	1 GB	50 (kB)
Tracker	10000000	1 GB	650
Preshower	145000	10 MB	50
ECAL	85000	10 MB	100
HCAL	14000	100 kB	50
Muon DT	200000	10 MB	10
Muon RPC	200000	10 MB	5
Muon CSC	400000	10 MB	90
Trigger		1 GB	16

Event size Max LV1 Trigger Online rejection System dead time 1 Mbyte 100 kHz 99.999% ~%