Intel® Array Building Blocks

Productivity, Performance, and Portability with Intel® Parallel Building Blocks

Intel SW Products Workshop 2010 CERN openlab

Optimization Notice



Software & Services Group, Developer Products Division

11/29/2010

Copyright© 2010, Intel Corporation. All rights reserved. *Other brands and names are the property of their respective owners.

Agenda

Part A - Introduction into Intel ArBB	3 hours
 Intel ArBB Overview, and Q&A LAB 1: "scalar", "scoped_timer" 	60m 45m
 Functions and Kernels, Containers and Parallelism LAB 2: "binding", "range", "for_vs_map" 	15m 60m
Part B - Advanced Topics	4 hours
 User-defined Types and Memory Model LAB 1: "complex", "interval" 	10m 50m
 Performance Optimization Hints LAB 2: "matrix_vector", "closure", "meta" 	15m 60m
 Software Design Aspects LAB 3: "heat", Demo(s)/Break 	05m 40m
 Intel ArBB Virtual Machine API IAB 4: "scalar ym" 	10m
 ArBB Release Schedule (KNF etc.) 	20m 10m
– Summary, Contact/Feedback, Q&A	20m



Software & Services Group, Developer Products Division

Optimization Notice

 \triangleright

Legal Information

- INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. NO LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE, TO ANY INTELLECTUAL PROPETY RIGHTS IS GRANTED BY THIS DOCUMENT. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY, RELATING TO SALE AND/OR USE OF INTEL® PRODUCTS INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.
- Intel may make changes to specifications and product descriptions at any time, without notice.
- All products, dates, and figures specified are preliminary based on current expectations, and are subject to change without notice.
- Intel, processors, chipsets, and desktop boards may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available on request.
- Any code names and other code names featured are used internally within Intel to identify products that are in development and not yet publicly announced for release. Customers, licensees and other third parties are not authorized by Intel to use code names in advertising, promotion or marketing of any product or services and any such use of Intel's internal code names is at the sole risk of the user
- Performance tests and ratings are measured using specific computer systems and/or components and reflect the
 approximate performance of Intel products as measured by those tests. Any difference in system hardware or software
 design or configuration may affect actual performance.
- Intel, Intel® Streaming SIMD Extensions (Intel® SSE), Intel® Advanced Vector Extensions (Intel® AVX), Intel® Parallel Building Blocks (Intel® PBB), Intel® Threading Building Blocks (Intel® TBB), Intel® Array Building Blocks (Intel® ArBB), Intel® Math Kernel Library (Intel® MKL), Intel® Integrated Performance Primitives (Intel® IPP), Intel® Cilk Plus and the Intel logo are trademarks of Intel Corporation in the United States and other countries.
- *Other names and brands may be claimed as the property of others.
- Copyright ©2010 Intel Corporation.



Copyright© 2010, Intel Corporation. All rights reserved. *Other brands and names are the property of their respective owners.

Optimization Notice

Intel[®] compilers, associated libraries and associated development tools may include or utilize options that optimize for instruction sets that are available in both Intel[®] and non-Intel microprocessors (for example SIMD instruction sets), but do not optimize equally for non-Intel microprocessors. In addition, certain compiler options for Intel compilers, including some that are not specific to Intel micro-architecture, are reserved for Intel microprocessors. For a detailed description of Intel compiler options, including the instruction sets and specific microprocessors they implicate, please refer to the "Intel[®] Compiler User and Reference Guides" under "Compiler Options". Many library routines that are part of Intel[®] compiler products are more highly optimized for Intel microprocessors than for other microprocessors. While the compilers and libraries in Intel[®] compiler products offer optimizations for both Intel and Intel-compatible microprocessors, depending on the options you select, your code and other factors, you likely will get extra performance on Intel microprocessors.

Intel[®] compilers, associated libraries and associated development tools may or may not optimize to the same degree for non-Intel microprocessors for optimizations that are not unique to Intel microprocessors. These optimizations include Intel[®] Streaming SIMD Extensions 2 (Intel[®] SSE2), Intel[®] Streaming SIMD Extensions 3 (Intel[®] SSE3), and Supplemental Streaming SIMD Extensions 3 (Intel[®] SSSE3) instruction sets and other optimizations. Intel does not guarantee the availability, functionality, or effectiveness of any optimization on microprocessors not manufactured by Intel. Microprocessor-dependent optimizations in this product are intended for use with Intel microprocessors.

While Intel believes our compilers and libraries are excellent choices to assist in obtaining the best performance on Intel[®] and non-Intel microprocessors, Intel recommends that you evaluate other compilers and libraries to determine which best meet your requirements. We hope to win your business by striving to offer the best performance of any compiler or library; please let us know if you find we do not.

Notice revision #20101101



Software & Services Group, Developer Products Division



Contact

Hans Pabst, Software Engineer TCE Performance and Productivity Libraries hans.pabst@intel.com



Software & Services Group, Developer Products Division

Optimization Notice

Copyright© 2010, Intel Corporation. All rights reserved. *Other brands and names are the property of their respective owners.





Software & Services Group, Developer Products Division

11/29/2010 6 11/29/2010

Copyright© 2010, Intel Corporation. All rights reserved. *Other brands and names are the property of their respective owners.

Optimization Notice

6